We claim:

1. A digital to analog converter (DAC) comprising:

a first capacitance and a second capacitance configured in a first switching circuit;

wherein the first switching circuit is configured as an input capacitance of a switched capacitor integrator;

wherein the first switching circuit is operable to redistribute charge stored on the first capacitance, to be shared substantially equally by the first capacitance and the second capacitance;

wherein the first switching circuit is further operable to redistribute charge stored on the second capacitance, to be shared substantially equally by the first capacitance and the second capacitance;

wherein applying a first-pass switching sequence to the first switching circuit for converting a binary number results in a first voltage across the first capacitance and across the second capacitance;

wherein applying a complementary switching sequence corresponding to the first-pass switching sequence to the first switching circuit for converting the binary number results in a second voltage across the first capacitance and across the second capacitance;

wherein, in applying the first-pass switching sequence, the first capacitance is charged to a conversion level a first number of times and the second capacitance is charged to the conversion level a second number of times;

wherein in applying the complementary switching sequence, the first capacitance is charged to the conversion level the second number of times and the second capacitance is charged to the conversion level the first number of times;

wherein, in applying the first-pass switching sequence, if the first capacitance is charged to the conversion level for a respective bit of the binary number then the second capacitance is not charged to the conversion level for the respective bit, and in applying the complementary switching sequence the first capacitance is not charged to the conversion level for the respective bit, but the second capacitance is;

wherein, in applying the first-pass switching sequence, if the second capacitance is charged to the conversion level for the respective bit, then the first capacitance is not charged to the conversion level for the respective bit, and in applying the complementary switching sequence the second capacitance is not charged to the conversion level for the respective bit, but the first capacitance is;

wherein the first-pass switching sequence and the corresponding complementary switching sequence form a conversion sequence for the binary number, wherein for each bit of the binary number, charge is redistributed between the first capacitance and the second capacitance;

wherein an integrated sum of the first voltage and the second voltage comprises a DAC output voltage free of odd-order errors, wherein if the first voltage is obtained from the first capacitance then the second voltage is obtained from the second capacitance, and if the first voltage is obtained from the second capacitance then the second voltage is obtained from the first capacitance;

wherein performing the conversion sequence a specified number of times and integrating the DAC output voltage at the end of each conversion sequence results in a final DAC output voltage;

wherein the final DAC output voltage is free of odd-order capacitor mismatch errors; and

wherein the final DAC output voltage is free of second-order capacitor mismatch errors for up to a specified number of bits.

2. The DAC of claim 1;

wherein the switched capacitor integrator comprises a first operational transconductance amplifier (OTA); and

wherein the first switching circuit is coupled to an inverting input of the first OTA.

3. The DAC of claim 1, further comprising a hold circuit coupled to an output of the switched capacitor integrator, wherein the hold circuit is operable to hold the final DAC output voltage.

4. The DAC of claim 3, wherein the hold circuit comprises:

a second OTA; and

a hold capacitor coupled to a non-inverting input of the second OTA;

wherein the output of the switched capacitor integrator is coupled to the non-inverting input of the second OTA.

5. The DAC of claim 1, wherein a value of the first capacitance is substantially the same as a value of the second capacitance.

6. The DAC of claim 1;

wherein if a bit value for the respective bit is 1, then the conversion level is a reference voltage; and

wherein if the bit value for the respective bit is 0, then the conversion level is common ground.

7. A method for digital to analog conversion of a binary number, the method comprising:

performing a conversion sequence a specified number of times, wherein the conversion sequence comprises:

applying a first-pass switching sequence to a first switching circuit comprising a first capacitance and a second capacitance, resulting in a first voltage across the first capacitance and across the second capacitance;

integrating the first voltage;

applying a complementary switching sequence corresponding to the first-pass switching sequence to the first switching circuit, resulting in a second voltage across the first capacitance and across the second capacitance; and

integrating the second voltage;

wherein if during said integrating the first voltage, the first voltage is obtained from the first capacitance then during said integrating the second voltage, the second voltage is obtained from the second capacitance, and if during said integrating the first

voltage, the first voltage is obtained from the second capacitance then during said integrating the second voltage, the second voltage is obtained from the first capacitance;

wherein said applying the first-pass switching sequence comprises charging the first capacitance to a conversion level a first number of times and charging the second capacitance to the conversion level a second number of times;

wherein said applying the complementary switching sequence comprises charging the first capacitance to the conversion level the second number of times and charging the second capacitance to the conversion level the first number of times;

wherein, if charging the first capacitance in said applying the first-pass switching sequence is performed for a respective bit of the binary number, then charging the second capacitance in said applying the first-pass switching sequence is not performed for the respective bit, and charging the first capacitance in said applying the complementary switching sequence is not performed for the respective bit, but charging the second capacitance in said applying the complementary switching sequence is performed;

wherein, if charging the second capacitance in said applying the first-pass switching sequence is performed for the respective bit, then charging the first capacitance in said applying the first-pass switching sequence is not performed for the respective bit, and charging the second capacitance in said applying the complementary switching sequence is not performed for the respective bit, but charging the first capacitance in said applying the complementary switching sequence is performed;

wherein said applying the first-pass switching sequence and said applying the complementary switching sequence each comprise redistributing charge stored on the first capacitance and the second capacitance to be shared substantially equally between the first capacitance and the second capacitance for each bit of the binary number;

wherein said performing the conversion sequence the specified number of times results in a final DAC output voltage;

wherein the final DAC output voltage is free of odd-order capacitor mismatch errors; and

wherein the final DAC output voltage is free of second-order capacitor mismatch errors for up to a specified number of bits.

8. The method of claim 7, wherein a value of the first capacitance is substantially the same as a value of the second capacitance.

9. The method of claim 7;

wherein if a bit value for the respective bit is 1, then the conversion level is a reference voltage; and

wherein if the bit value for the respective bit is 0, then the conversion level is common ground.

10. The method of claim 7;

wherein the first number is different for each conversion sequence in said performing the conversion sequence a specified number of times; and

wherein the second number is different for each conversion sequence in said performing the conversion sequence a specified number of times.

11. A method for operating a DAC for converting a binary number comprising one or more bits, wherein the DAC comprises a switched capacitor integrator and a first switching circuit comprising a first capacitor and a second capacitor of substantially equal values configured in parallel, wherein the first switching circuit is configured as an input capacitance of the switched capacitor integrator, the method comprising:

performing a conversion sequence a specified number of times, resulting in a final DAC output voltage and a corresponding final output charge, the conversion sequence comprising;

selecting a first subset of the one or more bits and a second subset of the one or more bits, wherein the first subset and the second subset are mutually exclusive, and wherein a union of the first subset and the second subset equal the one or more bits;

performing a first charging sequence for each bit of the first subset;

performing a second charging sequence for each bit of the second subset;

integrating a first output voltage present across the first capacitor, resulting in a first intermediate DAC output voltage and a corresponding first output charge;

performing the first charging sequence for each bit of the second subset; and

performing the second charging sequence for each bit of the first subset;

integrating a second output voltage present across the second capacitor, resulting in a second intermediate DAC output voltage and a corresponding second output charge;

wherein the first charging sequence comprises:

charging the first capacitor to a conversion voltage level resulting in a first conversion charge on the first capacitor;

redistributing the first conversion charge and a first previous charge present on the second capacitor between the first capacitor and the second capacitor;

wherein the second charging sequence comprises:

charging the second capacitor to a conversion voltage level resulting in a second conversion charge on the second capacitor;

redistributing the second conversion charge and a second previous charge present on the first capacitor between the first capacitor and the second capacitor;

wherein the final DAC output voltage is free of odd-order capacitor mismatch errors between the first capacitor and the second capacitor;

wherein the final DAC output voltage is free of second-order capacitor mismatch errors between the first capacitor and the second capacitor, for up to a specified number of bits.

12. The method of claim 11;

wherein for a bit value of 1 the conversion level is a reference voltage; and

wherein for a bit value of 0 the conversion level is a common ground.

13. The method of claim 11;

wherein the first subset is uniquely different for each conversion sequence of said performing the conversion sequence the specified number of times; and

wherein the second subset is uniquely different for each conversion sequence of said performing the conversion sequence the specified number of times.

14. The method of claim 11 further comprising:

transferring the final DAC output voltage to a hold circuit coupled to the switched capacitor integrator; and

holding the final DAC output voltage on the hold circuit.

15. The method of claim 11;

wherein performing the first charging sequence comprises performing the first charging sequence from LSB to MSB; and

wherein performing the second charging sequence comprises performing the second charging sequence from LSB to MSB.

16. The method of claim 11;

wherein said selecting the first subset a specified number of times and said selecting the second subset a specified number of times are performed in a manner that even-order capacitor mismatch errors are minimized in order of priority from MSB to LSB.

17. The method of claim 11;

wherein said selecting the first subset a specified number of times and said selecting the second subset a specified number of times are performed in a manner that second-order capacitor mismatch errors are eliminated in order of priority from MSB to LSB down to a specified number of bits.

18. The method of claim 11;

wherein the conversion sequence further comprises transferring the second output charge to the first capacitor and the second capacitor.

19. The method of claim 11 further comprising transferring the final output charge to the first capacitor and the second capacitor, resulting in a new final DAC output voltage.

20. The method of claim 19 further comprising:

transferring the new final DAC output voltage to a hold circuit coupled to the switched capacitor integrator; and

holding the new final DAC output voltage on the hold circuit.